IN THE SPECIFICATION

Please replace the paragraph on page 2 lines 30-31, corresponding to paragraph [0016], with the following amended paragraph:

The thin film transistor array panel may further include a redundant signal data line formed on the passivation layer and extending along the data line, and the passivation layer preferably has a contact hole for connection between the data line and the redundant signal data line.

Please replace the paragraph on page 6 lines 10-17, corresponding to paragraph [0044], with the following amended paragraph:

The data lines 171 for transmitting data voltages extend substantially in the longitudinal direction and intersect the gate lines 121 and the common electrode lines 131. Each pixel electrode lines 172 extend substantially in the longitudinal direction and includes a plurality of branches 174a-174c called pixel electrodes. The pixel electrodes 174a and 174b extend parallel to the common electrodes 133a and 133b respectively, and the pixel electrode 174c extends along the common electrode line 131 and is bifurcated into two branches parallel to the common electrodes 133a and 133b, respectively. Further, as shown in FIGS. 1-4, the distance between the common electrode (133a, 133b) and an adjacent pixel electrode (174a, 174b) is greater than the respective width of the common electrode and the adjacent pixel electrode. More particularly, the distance between common electrode 133a and the adjacent pixel electrode 174a is greater than the width of either the common electrode 133a or the pixel electrode 174a.

Please replace the paragraph on page 10 lines 7-11, corresponding to paragraph [0060], with the following amended paragraph:

The disclination lines are generated near the areas where the orientations of the liquid crystal molecules vary. The molecular orientations shown in FIG. 1 vary only near the pixel electrode 174c, while those shown in FIGS. 10A and 10B vary near the three curves of the pixel electrodes. Accordingly, the number of the disclination lines shown in FIG. 1 is very small compared with those shown in FIGS. 10A and 10B.

Page 2 of 12

Appl. No. 10/656,065

LAW OFFICES OF PIAC PIERSON KYOK CHEN & HEID LLP 2402 MICHELSON DRIVE SUITE 210 IRVINE CA. 92612 (949) 132-7040 FAX (403) 392-9262 Please replace the paragraph on page 11 lines 8-10, corresponding to paragraph [0068], with the following amended paragraph:

Subsequently, a plurality of [[date]] <u>data</u> lines 171 including a plurality of source electrodes 173 and a plurality of pixel electrode lines 172 including a plurality of drain electrodes 175 and a plurality of pixel electrodes <u>1</u>74a-<u>1</u>74c are formed.

Please replace the ABSTRACT OF THE DISCLOSURE with the following amended ABSTRACT OF THE DISCLOSURE:

A thin film transistor array panel is provided, which includes: a gate line and a data line formed on an insulating substrate and intersecting each other; a plurality of common electrodes separated from the gate line and the data line and making an angle of about 7-23 degrees with the gate line; a plurality of pixel electrodes separated from the gate line, the data line, and the common electrodes, extending parallel to the common electrodes, and alternately arranged with the common electrodes; and a thin film transistor connected to the gate line, the data line, and the pixel electrodes, wherein the distance between the common electrode and the pixel electrode is greater than the respective width of the common electrode and the pixel electrode.

Lan offices of Nacphieson Kwok Chen a Bed Lif 2402 Michelson Drivs Suite 210 Irvine Ca. 92412 (49) 752-7040 Fax (405) 772-7252

Page 3 of 12

Appl. No. 10/656,065